11-22-00

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Case Docket No. PHN 17,746

THE COMMISSIONER FOR PATENTS, Washington, D.C. 20231

Enclosed for filing is the patent application of Inventor(s):
MARTIJN JOHANNES LAMBERTUS EMONS

For: DATA PROCESSING UNIT WITH ACCESS TO THE MEMORY OF ANOTHER DATA PROCESSING UNIT DURING STANDBY

ENCLOSED ARE:

[X] Appointment of Associates;
[X] Information Disclosure Statement, Form PTO-1449 and copies of documents listed therein;
[X] Preliminary Amendment;
[X] Specification (8 Pages of Specification, Claims, & Abstract);
[X] Declaration and Power of Attorney:
(2 Pages of a [ ]fully executed [X]unsigned Declaration);
[X] Drawing (2 sheets of [ ]informal [X]formal sheets);
[X] Certified copy of a EUROPEAN application Serial No.99203936.2;
[X] Authorization Pursuant to 37 CFR §1.136(a)(3)
[ ] Other: ;
[ ] Assignment to .

FEE COMPUTATION

CLAIMS AS FILED				
FOR	NUMBER FILED	NUMBER EXTRA	RATE	BASIC FEE - $710.00
Total Claims	8 - 20 =	0	X $18 =	0.00
Independent Claims	2 - 3 =	0	X $80 =	0.00
Multiple Dependent Claims, if any			$270 =	0.00
TOTAL FILING FEE			=	$710.00

Please charge Deposit Account No. 14-1270 in the amount of the total filing fee indicated above, plus any deficiencies. The Commissioner is also hereby authorized to charge any other fees which may be required, except the issue fee, or credit any overpayment to Account No. 14-1270.

[ ]Amend the specification by inserting before the first line as a centered heading --Cross Reference to Related Applications--; and insert below that as a new paragraph --This is a continuation-in-part of application Serial No. , filed , which is herein incorporated by reference--.

CERTIFICATE OF EXPRESS MAILING

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Date of Deposit November 21, 2000
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IN THE UNITED STATE PATENT TRADEMARK OFFICE

IN re APPLICATION OF ATTY. DOCKET

MARTIJN JOHANNES LAMBERTUS EMONS PHN 17,746

Serial No. Group Art Unit

Filed: CONCURRENTLY Ex.

Title: DATA PROCESSING UNIT WITH ACCESS TO THE MEMORY OF ANOTHER DATA PROCESSING UNIT DURING STANDBY

Commissioner for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

Prior to calculation of the filing fee and examination, please amend the above-identified application as follow:

IN THE CLAIMS

Please amend the claims as follows:

Claim 3, line 1, delete "or 2"

Claim 4, line 1, delete "2 or 3,"

Claim 5, line 1, delete "2, 3, or 4,"

Claim 6, line 1, delete "2, 3, or 4,"

Claim 7, line 1 delete "2 or 3,"

REMARKS

The claims have been amended to delete multiple dependencies.

The within amendment is limited to the equivalent of cancellation of claims, and pursuant to MPEP §506, should be entered prior to calculation of the fee.

Respectfully submitted,

By ______________________

Jack D. Slobod, Re. 26,236
(914) 333-9606
November 19, 2000

Data processing unit with access to the memory of another data processing unit during standby.

The invention relates to a data processing system which may be situated in a reduced-power mode, comprising a first data processing unit that has access to a memory belonging to the first data processing unit and a second data processing unit that has access to the memory belonging to the first data processing unit.

The invention also relates to a data processing unit that may be situated in a reduced-power mode and has access to a memory belonging to the data processing unit.

An arrangement of this type is known from WO 99/00741. A multifunction controller is described herein to be used in a personal computer, which includes a unified graphics/video controller. The unified graphics/video controller processes the data intended for the user into a signal that is suitable for reproduction by a display unit. The data for the unified video controller is supplied by the CPU (Central Processing Unit). The CPU can write the data in the memory belonging to the unified graphics/video controller, supply it via a register structure or render it available in the memory belonging to the CPU after which the unified graphics/video controller can fetch the data from the memory belonging to the CPU. After the unified graphics/video controller has the data at its disposal, it is processed by means of the memory belonging to the unified graphics/video controller. In WO 99/00741, the exchange of this data is effected by a communication link and a combined PCI bridge and a cache controller as a result of which the unified graphics/video controller has access to the cache memory that belongs to the CPU.

A disadvantage of this arrangement is that when a picture is still to be reproduced via the unified graphics/video controller in a reduced-power mode of the system, an unnecessarily large part of the data processing system is to remain active, leading to an unnecessarily large energy consumption.

It is an object of the invention to further reduce the energy consumption of a reduced-power mode data processing unit by efficiently utilizing the available system components.

For this purpose, the arrangement according to the invention is characterized in that the first data processing unit is arranged for offering the second data processing unit access to the memory belonging to the first data processing unit in a reduced-power mode of the data processing system.

In a reduced-power mode of the data processing system, the second data processing unit is often to process information, it is true, but the quantity and exchange of information is usually limited. The first data processing unit is only to execute a reduced number of tasks in the reduced-power mode, so that part of the memory belonging to the first data processing unit remains unused. By using the memory belonging to the first data processing unit for storing data of the second data processing unit in the reduced-power mode, the use of the second data processing unit's own memory may be avoided and the system components can be made optimum use of.

The memory belonging to the first data processing unit may furthermore fit better as regards capacity with the quantity of data produced in the reduced-power mode and to be processed by the second data processing unit, or may form part of a system component that is not used in the reduced-power mode, but is not switched off either. If the second data processing unit is to process data only in the reduced-power mode, a memory of its own for the second data processing unit may be omitted.

All this results in an efficient use of the available system components and reduced energy consumption.

An embodiment of the invention is characterized in that the first data processing unit is arranged for offering access to the memory belonging to the first data processing unit during a reduced-power mode of the first data processing unit.

For the time when the first data processing unit is situated in a reduced-power mode, the memory belonging to the first data processing unit is normally not used. By utilizing this unused memory, the use of the second data processing unit's own memory is avoided, which results in an efficient use of the system components and reduced energy consumption.

A further embodiment of the invention is characterized in that the first data processing unit is arranged for offering access to the memory belonging to the first data processing unit to the second data processing unit when a memory belongs to the second data processing unit is switched off.

In the reduced-power mode, as many components as possible of the data processing system are to be switched off to provide optimum energy consumption. By switching off the memory belonging to the second data processing unit in the reduced-power mode and offering the second data processing unit access to the memory belonging to the first data processing unit, the energy consumption of the data processing system is reduced and the second data processing unit may continue to execute a reduced set of tasks with the aid of the memory belonging to the first data processing unit. The memory belonging to the first data processing unit may, for example as regards capacity, fit better with the reduced quantity of data to be processed in the reduced-power mode, or be part of a system component that is not used in the reduced-power mode but is not switched off either.

The invention will be further explained with reference to drawings in which:

Fig. 1 represents a system in which a controller controls the interaction between the various system components;

Fig. 2 represents a system in which the video controller utilizes the external memory of a microprocessor;

Fig. 3 represents a system in which the video controller utilizes the internal memory of a microprocessor; and

Fig. 4 represents a system in which the video controller has the disposal of a memory of its own, but utilizes the memory of the microprocessor in the reduced-power mode.

In these Figures the data processing unit is shown in the form of a microprocessor. Other data processing units too, such as a digital signal processor, may be used.

Fig. 1 shows a data processing system comprising a microprocessor 10, a memory 15 belonging to the microprocessor, a controller 13 controlling the interaction between the system components and a video controller 17. This system may be situated in a reduced-power mode.

In the reduced-power mode it is important to make optimum use of the various system components. In the reduced-power mode the video controller 17 often reproduces a limited quantity of information. This requires a memory in which this information is stored. By utilizing the memory 17 belonging to the microprocessor 10, the use of a memory of its

own of the video controller 17 can be avoided. The microprocessor 10 in the reduced mode is less active or inactive, which results in a reduced use of the memory 15. The capacity of the memory 15 that is vacated may be used by the video controller 17. If the microprocessor 10 is switched off in the reduced-power mode, the whole part of the memory 15 that is assigned to the microprocessor 10 becomes available to the video controller 17.

When the video controller 17 reproduces data only in the reduced-power mode, the memory 15 will suffice as the sole memory for the video controller 17, because in the normal-power mode the video controller 17 does not need a memory and the memory 15 is thus again completely available to the microprocessor 10.

Fig. 2 shows a data processing system comprising a microprocessor 20, a video controller 27, an external memory 25 belonging to the microprocessor, and a controller 23 included in the microprocessor 20. The controller 23 controls, possibly commanded by the microprocessor 20, the access to the memory 25 belonging to the microprocessor 20. By keeping parts of the microprocessor 20, among which the controller 23, in an active state, so that the video controller 27 can utilize the memory 25 belonging to the microprocessor 20 in the reduced-power mode, the use of a memory of its own belonging to the video controller 27 can be avoided. In the reduced-power mode, for example, the microprocessor 20 can be switched off, whereas the access to the memory 25 is maintained for the video controller 27. As a result, the energy consumption is reduced and the system components are made optimum use of. When video controller 27 reproduces data only in the reduced-power mode, the memory 25 will suffice as the sole memory for the video controller 27, because the video controller 27 in the normal-power mode does not need any memory and the memory 25 is thus again completely at the disposal of the microprocessor 20.

Fig. 3 shows a data processing system comprising a video controller 27, a microprocessor 30 including a memory 35 inside the microprocessor 30, which memory is accessible to the video controller 37 from the exterior in the reduced-power mode. The microprocessor 30 is not switched off in some systems, but needs to execute only a minimum set of tasks. To this end, the microprocessor 30 needs to have only a small portion of the memory 35, whereas yet the whole memory 35 is to be supplied with energy. By allowing the video controller 37 to make use of the unused part of the memory 35, the use of an additional memory belonging to the video controller 37 can be avoided. As a result, also the energy consumption associated to the memory belonging to the video controller 17 is avoided and optimum use is made of the available system components.

Fig. 4 shows a data processing system comprising a microprocessor 40, a controller 43, a memory 45 belonging to the microprocessor, a video controller 47, a memory 49 belonging to the video controller 47, and a switch 48 for interrupting the energy supply to the memory 49.

In the reduced-power mode the controller 43 offers the video controller 47 access to the memory 45 belonging to the microprocessor 40. The memory 45 has sufficient storage capacity for the data of the video controller 47 in the reduced-power mode. The memory 49 belonging to the video controller 47 is no longer necessary in the reduced-power mode and can be switched off by a switch 49 or a power-down pin 46, so that there is a reduction of energy consumption. The switching-off of the memory 49 belonging to the video controller 47 may be combined with the improvements shown in Figs. 1, 2 and 3.

CLAIMS:

1. A data processing system which may be situated in a reduced-power mode, comprising a first data processing unit that has access to a memory belonging to the first data processing unit and a second data processing unit that has access to the memory belonging to the first data processing unit,
characterized in that the first data processing unit is arranged for offering the second data processing unit access to the memory belonging to the first data processing unit in a reduced-power mode of the data processing system.

2. A data processing system as claimed in claim 1,
characterized in that the first data processing unit is arranged for offering the second data processing unit access to the memory belonging to the first data processing unit in a period of time in which the reduced-power mode of the data processing system implies a reduced-power mode of the first data processing unit.

3. A data processing system as claimed in claim 1 or 2,
characterized in that the first data processing unit is arranged for offering the second data processing unit access to the memory belonging to the first data processing unit when a memory belonging to the second data processing unit is switched off.

4. A system as claimed in claim 1, 2 or 3,
characterized in that the memory belonging to the first data processing unit forms part of the first data processing unit.

5. A system as claimed in claim 1, 2, 3 or 4,
characterized in that the memory belonging to the first data processing unit is a cache memory.

6. A system as claimed in claim 1, 2, 3 or 4,
characterized in that the first data processing unit is a microprocessor.

7. A system as claimed in claim 1, 2 or 3, characterized in that the second data processing unit is a video controller.

8. A data processing unit having access to a memory belonging to the data processing unit which data processing unit may be situated in a reduced-power mode, characterized in that the data processing unit is arranged for offering access in the reduced-power mode to the memory belonging to the data processing unit.

ABSTRACT:

In a reduced power mode a first data processing unit forming part of a data processing system offers a second data processing unit access to its associated memory in order to optimize the use of energy and available resources. The first data processing unit requires reduced storage space in the reduced power mode, which remaining storage space can be made available to the second data processing unit. The memory associated to the second data processing unit can be switched off to save energy, or can be removed altogether if the second data processing unit only operates in the reduced power mode.

Fig. 1

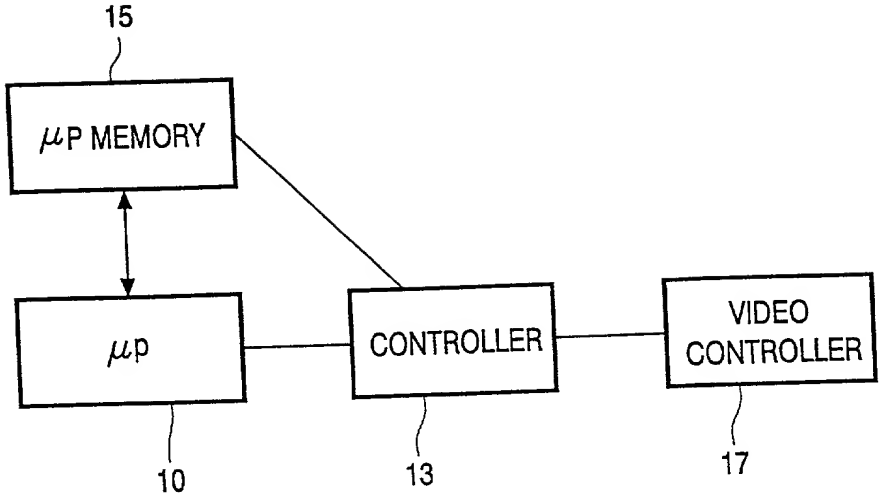

FIG. 1

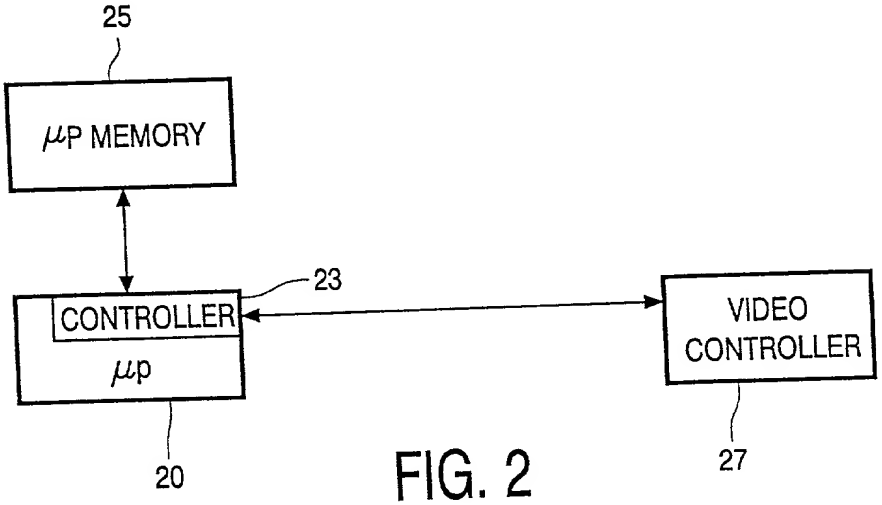

FIG. 2

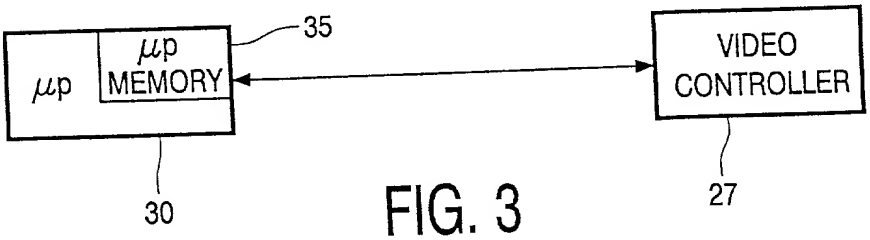

FIG. 3

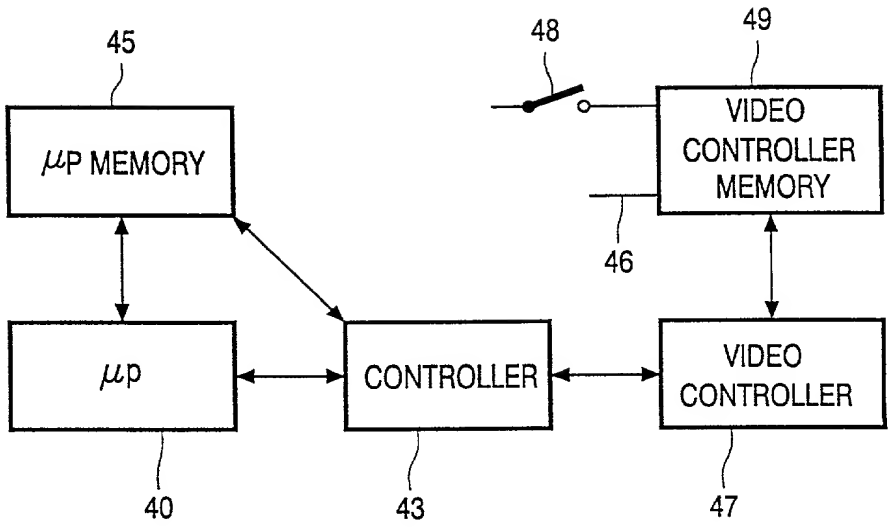

FIG. 4

DECLARATION and POWER OF ATTORNEY

ATTORNEY'S DOCKET NO.:
PHN 17.746

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

"Data processing unit with access to the memory of another data processing unit during standby"

the specification of which (check one)

☐ is attached hereto.

☐ was filed on _____ as Application Serial No. _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by the amendment(s) referred to above.

I acknowledge the duty to disclose information which is material to patentability of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

PRIOR FOREIGN APPLICATION(S)

COUNTRY	APP. NUMBER	DATE OF FILING (DATE, MONTH, YEAR)	PRIORITY CLAIMED UNDER 35 U.S.C. 119
Europe	**99203936.2**	**24 November 1999**	**YES**

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35 United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1,56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

PRIOR UNITED STATES APPLICATION(S)

APPLICATION SERIAL NUMBER	FILING DATE	STATUS (PATENTED, PENDING, ABANDONED)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (list name and registration number)

Jack E. Haken, Reg. No. 26,902

Michael E. Marion, Reg. No. 34,266

Edward M. Blocker, Reg. No. 30,245

SEND CORRESPONDENCE TO: Corporate Patent Counsel;	DIRECT TELEPHONE CALLS TO:
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Dated:		Inventor's Signature:		
Full Name of in Inventor	Last Name **EMONS**	First Name **Martijn**	Middle Name **Johannes Lambertus**	
Residence & Citizenship	City **Nijmegen**	State of Foreign Country **The Netherlands**	Country of Citizenship **The Netherlands**	
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of | Atty. Docket
MARTIJN JOHANNES LAMBERTUS EMONS | PHN 17,746

Serial No. | Group Art Unit

Filed: CONCURRENTLY | Ex.

Title: DATA PROCESSING UNIT WITH ACCESS TO THE MEMORY OF ANOTHER DATA PROCESSING UNIT DURING STANDBY

Commissioner for Patents
Washington, D.C. 20231

APPOINTMENT OF ASSOCIATES

Sir:

The undersigned Attorney of Record hereby revokes all prior appointments (if any) of Associate Attorney(s) or Agent(s) in the above-captioned case and appoints:

JACK D. SLOBOD **(Registration No. 26,236)**

c/o U.S. PHILIPS CORPORATION, Intellectual Property Department, 580 White Plains Road, Tarrytown, New York 10591, his Associate Attorney(s)/Agent(s) with all the usual powers to prosecute the above-identified application and any division or continuation thereof, to make alterations and amendments therein, and to transact all business in the Patent and Trademark Office connected therewith.

ALL CORRESPONDENCE CONCERNING THIS APPLICATION AND THE LETTERS PATENT WHEN GRANTED SHOULD BE ADDRESSED TO THE UNDERSIGNED ATTORNEY OF RECORD.

Respectfully,

Jack E. Haken, Reg. 26,902
Attorney of Record

Dated at Tarrytown, New York
this 19th day of November, 2000.
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